IN THE SPECIFICATION:

Please amend paragraph **[0001]** as follows:

[0001] This application is a divisional of application Serial No. 09/933,297, filed August 20, 2001, ~~pending.~~ now U.S. Patent 6,967,125, issued November 22, 2005.

Please amend paragraph **[0005]** as follows:

[0005] In an effort to increase the number of connections in an integrated circuit (IC) package while maintaining or decreasing the overall size, alternative packaging arrangements have been implemented. For example, grid array devices such as pin grid arrays ~~(PGA's),~~ (PGAs), ball grid arrays ~~(BGA's),~~ (BGAs), (land grid arrays ~~(LGA's)~~ (LGAs) and their associated variants have been used to reduce package size and increase input/output connections. As an example of a grid array type device, a BGA device employs a number of input/output connections in the form of conductive bumps, such as solder balls, extending transversely from a major surface of the package in a pattern, or "array," of columns and rows. The conductive bumps may be formed on one surface of a circuit board or other interposer substrate and are in electrical connection with bonding pads on the opposing surface of the circuit board. A semiconductor die is coupled to the bonding pads, such as by wire bonding, to establish electrical connections from the bond pads of the semiconductor die to the conductive bumps. The resulting assembly is then typically ~~encapsulated~~ encapsulated, such as by transfer molding with a filled ~~polymer~~ polymer, with the array of conductive bumps being left exposed for subsequent electrical connection to ~~higher-level~~ higher-level packaging such as a carrier substrate. The conductive bumps are configured to be coupled to a mirror image pattern of terminal pads on the carrier substrate which may comprise a printed circuit board (PCB) or another structure by reflowing the solder. In essence, a BGA device increases the number of input/output connections by allowing the connections to be positioned over substantially the entirety of a major surface of the package rather than extending laterally outwardly from the periphery of the package such as in a QFP.

Please amend paragraph **[0009]** as follows:

[0009] One aspect of the invention includes a method of forming a semiconductor die or IC package. The method includes providing a semiconductor die having a plurality of bond pads located on an active surface thereof. A lead frame having a plurality of conductive leads is provided adjacent the semiconductor die. A first bond ~~bad~~ pad on the semiconductor die is electrically coupled to a first portion of at least one conductive lead and a second bond pad is coupled to a second portion of the same lead. The first portion and second portion of the lead are then electrically isolated from one another to form two individual conductive elements from the original conductive lead. Additionally, an insulative encapsulant may be formed about the semiconductor die and at least partially about the lead frame while allowing a portion of each individual conductive element to remain exposed for subsequent electrical coupling with an external electrical circuit such as a carrier substrate.

Please amend paragraph **[0015]** as follows:

[0015] In accordance with another aspect of the invention, another IC package is provided. The IC package includes a semiconductor die having a plurality of bond pads and a lead frame having a plurality of conductive leads. Each of the plurality of conductive leads is electrically coupled to at least two bond pads of the plurality of bond pads.

Please amend paragraph **[0022]** as follows:

[0022] FIGS. 4A and 4B are partial plan views of an IC package according to alternative embodiments;

Please amend paragraph **[0025]** as follows:

[0025] FIGS. 1 and 2 depict one embodiment of an IC package of the present invention in the form of a quad flat no-lead (QFN) grid array package 10. FIG. 1 presents a view of a major surface comprising the underside of the QFN package 10, while FIG. 2 shows a ~~cross section~~ cross-section of the QFN package 10 taken along section line 2-2 as shown in FIG. 1.

The QFN package 10 includes a semiconductor die 12 positioned on and secured by its back side to a die paddle 14, die paddle 14 originally comprising a portion of a lead frame as will be hereinafter described. Conductive elements 16 are positioned about the die paddle 14 in a grid array pattern, outwardly of semiconductor die 12 and adjacent the lateral periphery of QFN package 10. The die paddle 14 and conductive elements 16 may be formed of any suitable material such as copper, aluminum, alloy 42 or any other suitable conductive material for lead frames as understood by those of ordinary skill in the art.

Please amend paragraph **[0026]** as follows:

[0026] The grid array pattern of the conductive elements 16 may be described in various geometrical terms such as a grid having a specified number of columns and rows. However, due to the general placement of the conductive elements 16 outwardly of the semiconductor die 12 and generally adjacent the lateral periphery of the QFN package 10, the grid array structure will be discussed in terms of peripheral rows. Thus, the QFN package 10 shown in FIGS. 1 and 2 includes a first inner peripheral row 18A and a second outer peripheral row 18B of conductive elements 16.

Please amend paragraph **[0027]** as follows:

[0027] The language "peripheral row" is used herein for convenience in describing the configuration of the QFN package 10 and should not be understood as requiring all of the conductive elements 16 to be located at or on the lateral peripheral edge of the QFN package 10, nor should such phraseology be taken to mean that a given lateral peripheral row of conductive elements 16 must circumscribe the entire die paddle 14 and semiconductor die 12. While it is desirable to have the conductive elements 16 positioned about each side of the QFN package 10 so as to maximize the number of conductive elements 16 in the package, some designs may not require such an arrangement. Alternatively, some configurations may include lateral peripheral rows that only partially circumscribe the die paddle 14 and semiconductor die 12, such as arrangements where lateral peripheral rows lie on opposing sides of the QFN package 10.

Please amend paragraph **[0028]** as follows:

[0028] The conductive elements 16 are each conductively coupled to a bond pad 22 on the active surface of semiconductor die 12 such as by wire bonds 24. The semiconductor die 12 and wire bonds 24 are encapsulated with an electrically insulative (dielectric) material 26 which also partially encapsulates the conductive elements 16 and extends between die paddle 14 and the inner peripheral row 18A of conductive elements 16, between the inner peripheral row 18A of conductive elements 16 and the outer peripheral row 18B of conductive elements 16 and between laterally adjacent conductive elements 16 of each of the inner and outer peripheral rows 18A and 18B, respectively. The encapsulant material 26 may comprise a silicon particle-filled polymer encapsulant applied under heat and pressure by transfer molding, as well known in the art.

Please amend paragraph **[0029]** as follows:

[0029] The conductive elements 16 each have an exposed surface 28 on the bottom major surface of the QFN package 10 for subsequent electrical coupling with another electrical component such as a carrier substrate (not shown). Such connection may be made, for example, through the use of conductive bumps 28b, shown in broken lines for clarity. Such bumps may include, for example, solder bumps which are stenciled onto conductive elements 16 and then reflowed to form balls, conductive or conductor-filled epoxy columns or pillars, or ~~self-supporting~~ self-supporting spheres (either conductive or insulative) covered with a conductive material. It is further contemplated that an anisotropic, so-called "Z-axis" conductive material comprising ~~laterally spaced~~ laterally spaced conductive elements in a dielectric film and oriented transversely to the plane thereof may also be employed to connect conductive elements 16 to a carrier substrate. All of the foregoing approaches, and others, are known to those of ordinary skill in the art and are not to be taken as limiting of the present invention.

Please amend paragraph **[0030]** as follows:

[0030] The inner peripheral rows 18A and outer peripheral rows 18B of conductive elements 16 adjacent each edge of QFN package 10 are shown to be separated from one another by an elongated, trough-like concavity or recess 30. As shown in FIG. 2, the concavity or recess 30 is formed as an elongated saw cut or scribe line extending from a first lateral edge of the QFN package 10 to an opposing lateral edge. However, the concavity may be formed according to other techniques known in the art such as, for example, a masking and etching process. In the embodiment shown in FIGS. 1 and 2, the concavity or recess 30 serves to create the individual conductive elements 16 of the two inner and outer peripheral rows 18A and 18B, respectively, from a single row of individual, laterally extending ~~leads~~ leads 16′ of a lead frame. The fabrication process can be seen more clearly with reference to FIGS. 3A and 3B. FIG. 3A depicts a partial section of the QFN package 10 showing the QFN package 10 at a stage in fabrication prior to formation of the individual conductive elements 16. The QFN package 10 shown in FIG. 3A includes a single lead 16′ rather than individual conductive elements 16. It is further noted that there are multiple wire bonds 24 connected to different bonding regions 32, 34 of the lead 16′. A severance region 36, shown as an upwardly facing notch, is preformed in the lead 16′ and subsequently filled with encapsulant 26 subsequent to attachment of semiconductor die 12 to die paddle 14 and wire bonding of a bond pad 22 (not shown in FIG. 3A) to bonding regions 32, 34. The notch of severance region 36 may be formed by various processes such as saw cutting, scribing, scoring or etching of the lead 16′ prior to encapsulation of the lead 16′ and wire bond 24 and preferably prior to attachment of semiconductor die 12 to die paddle 14.

Please amend paragraph **[0032]** as follows:

[0032] While the severance region 36 is desirably in the form of a notch or recess as shown, it is contemplated that the severance region 36 of the lead 16′ may simply be a designated area of separation without a notch or other physical feature. It is noted that, in such a case, the concavity or recess 30 extending upwardly from the bottom major surface of QFN package 10 would penetrate through the entire thickness of the lead 16′ and there would be no encapsulant 26

formed between the adjacent inner and outer individual conductive elements 16 to serve as a structural member 38. If desired, a structural member 38 could be formed after the formation of the concavity or recess 30 by filling the same with dielectric material regardless of whether or not an upwardly facing, preformed notch or recess in each lead 16′ is used to facilitate the formation of individual conductive elements 16.

Please amend paragraph **[0033]** as follows:

[0033] Referring to FIGS. 4A and ~~4B~~ 4B, alternative embodiments are shown with regard to the grid array pattern. FIG. 4A shows a portion of the bottom surface of a QFN package 10′ having three different peripheral rows 18A, 18B and 18C of conductive elements 16. The conductive elements 16 are formed in a manner similar to that described above except that additional severance regions 36 (or notches) would be located in each lead 16′ (see FIGS. 3A, 3B and 5) and that there are additional concavities or recesses 30 to assist in forming the third peripheral ~~rows~~ row 18C.

Please amend paragraph **[0034]** as follows:

[0034] FIG. 4B shows a partial section of the bottom surface of a QFN package 10″ also having three peripheral rows 18A′, 18B′ and 18C′. However, in the embodiment of FIG. 4B the conductive elements 16″ of the peripheral rows 18A′, 18B′ and 18C′ are staggered such that a conductive element 16″ in peripheral row 18B′ is shifted slightly to one side as compared to an adjacent conductive element 16″ in peripheral row 18A′. Similarly, a conductive element 16″ in peripheral row 18C′ is shifted slightly to one side as compared to an adjacent conductive element 16″ in peripheral row 18B′. Such an arrangement is possible by forming a lead frame having ~~leads 16′~~ leads positioned at an angle other than perpendicular with respect to an adjacent edge of the die paddle 14. The individual peripheral rows ~~18A′,18B′~~ 18A′, 18B′ and 18C′ are formed in a manner similar to that described above, with elongated, trough-like concavities or recesses 30 being formed to ultimately create the individual conductive elements 16″. The staggered configuration serves to allow more flexibility in wire bonding configurations and

potentially lower bond loop heights due to the lateral staggering of the individual conductive elements 16″. Thus, depending on the angle at which a lead 16′ is formed on a lead frame, the offset of one peripheral row 18′, 18B′ and 18C′, respectively, relative to another may be controlled and wire bonding configurations may be flexibly designed.

Please amend paragraph **[0035]** as follows:

[0035] Referring now to FIG. 5, an exemplary lead frame strip 50 including a plurality of individual lead frames 52 for use in forming QFN packages 10 is shown. The multiple lead frames 52 are formed in a single, longitudinally extending lead frame strip 50 as is known by those of ordinary skill in the art. Each lead frame 52 includes an outer frame portion 52o bearing a die paddle 14 supported substantially in the center thereof by tie bars and multiple inwardly extending, cantilevered leads 16′. A reduced number of leads 16′ is shown for clarity, but is not intended to be limiting of the invention. The leads 16′ are each formed with a severance region 36, such as a notch or similar recess, for subsequent formation of individual conductive elements 16 from the leads 16′. As discussed above, the severance regions 36 may be formed by various techniques such as scoring, saw cutting, or etching. The severance regions 36 define the locations of the peripheral rows 18A and 18B which will be subsequently formed in the QFN package 10. The lead frames 52 depicted in FIG. 5 are representative of a lead frame 52 which might be used in the formation of a QFN package 10 described in conjunction with FIGS. 1 and 2. Other lead frames of suitable configuration and with similar features would be utilized in forming the QFN packages 10′, 10″ discussed in conjunction with FIGS. 4A ~~or 4B respectively~~ or 4B, respectively, as is understood by those of ordinary skill in the art. In fabricating QFN packages of the present invention, the outer frame portions 52o are severed from the packages to effect electrical isolation of die paddle 14 as well as each set of conductive elements 16 from the outer frame portions 52o, while mutual electrical isolation between the conductive elements 16 formed from each lead 16′ is effected by cutting through the leads 16′ from the lead surfaces opposite the notches of severance regions 36. To facilitate alignment of the QFN packages for creating the concavities or recesses 30, it is preferred currently that QFN packages 10 be severed

from outer frame portions 52o after such concavities or recesses ~~are~~ 30 are cut or otherwise formed. If conductive bumps 28b (see FIG. 2) are to be formed or placed on conductive elements 16, it may also be desirable to form or place conductive bumps 28b while QFN packages 10 are still unsevered from lead frame strip 50 to facilitate alignment and handling.

Please amend paragraph **[0036]** as follows:

[0036] Referring now to drawing FIG. 6, a schematic of an electronic system 60, such as a personal computer, including an input device 62 (such as a keyboard and mouse) and an output device 64 (such as a display or printer interface) coupled or otherwise in electrical communication with a processor device 66, is illustrated. Processor device 66 is also coupled or otherwise in operable electrical communication such as through traces of a motherboard with one or more memory modules 68 incorporating a plurality of QFN packages according to the present invention such as 10, 10′, 10″ or variations thereof. The memory module 68 may include a memory board 70 having an electrical circuit formed therein, such as a ~~PCB.~~ printed circuit board (PCB). Furthermore, processor device 66 may be directly embodied in a module with a QFN package which incorporates the teachings hereof and may further include, without limitation, a microprocessor, a first level cache memory, and additional ICs, such as logic circuits, a video processor, an audio processor, or a memory management processor.

Please amend paragraph **[0037]** as follows:

[0037] While the present invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.